

**SPECIFICATION AMENDMENT**

1. Please replace paragraph [0001] with the following amended paragraph:

**CROSS-REFERENCE TO RELATED APPLICATIONS**

[0001] This application is related to U.S. patent application serial number 09/738,960, titled "Caching System and Method for a Network Storage System" by Lin-Sheng Chiou, Mike Witkowski, Hawkins Yao, Cheh-Suei Yang, and Sompong Paul Olarig, which was filed on December 14, 2000, now U.S. Patent No. 6,792,507, and which is incorporated herein by reference in its entirety for all purposes; U.S. patent application serial number 10/015,047, [attorney docket number 069099.0102/B2], titled "System, Apparatus and Method for Address Forwarding for a Computer Network" by Hawkins Yao, Cheh-Suei Yang, Richard Gunlock, Michael L. Witkowski, and Sompong Paul Olarig, which was filed on October 26, 2001 and which is incorporated herein by reference in its entirety for all purposes; ~~U.S. patent application serial number \_\_\_\_\_, titled "Network Processor to Switch Fabric Bridge Implementation" by Sompong Paul Olarig, Mark Lyndon Oelke, and John E. Jenne, which was filed on \_\_\_\_\_, and which is incorporated herein by reference in its entirety for all purposes;~~ U.S. patent application serial number 10/039,189, [attorney docket number 069099.0106/B6-A], titled "XON/XOFF Flow Control for Computer Network" by Hawkins Yao, John E. Jenne, and Mark Lyndon Oelke, which is being filed concurrently on December 31, 2001, and which is incorporated herein by reference in its entirety for all purposes; and U.S. patent application serial number 10/039,184, [attorney docket number 069099.0107/B6-B], titled "Buffer to Buffer Credit Flow Control for Computer Network" by John E. Jenne, Mark Lyndon Oelke and Sompong Paul Olarig, which is being filed concurrently on December 31, 2001, and which is incorporated herein by reference in its entirety for all purposes.

2. Please replace paragraph [0024] with the following amended paragraph:

[0024] Numeral 406a-e indicates the inbound data queues for each path. These queues 406a-e are coupled through a multiplexer 407 with a single queue 408 which is coupled with CSIX Tx interface 409. An arbitrator (not shown) is used to control the multiplexer. It arbitrates among the five inbound queues 406a-e in a round robin fashion. Each queue 406a-e and 408 can be implemented with a weighed priority scheme that will be described later and which may be monitored by the bridge system. In another exemplary embodiment, so-called watermark registers can be used to indicate the filling status of a queue. The ingress path also handles width and frequency matching between the interfaces as the data width of the CSIX Tx interface ~~[[109]]~~ 409 is twice as wide and twice as fast as that of each network processor interface 401a-e. The depth of the queues 406a-e can be configured depending on the overall system performance. The queues 406a-e and 408 can have, for example but not limited to, a depth of 10 cells for the ingress outbound queue to provide sufficient depth, thus minimizing unnecessary back pressure via Link-Level Flow Control caused by temporary over-subscription. This situation can take place in the unlikely event when all network processors operate at full speed. In this case the outbound speed of 64 bit width @ 200 MHz (equivalent to 32 bit width @ 400 MHz) will be overloaded by the five network processors (equivalent to 32 bit width @ 500 MHz). However, normally the network processor throughput is usually around 1000 MB/s for ten 1 Gbps fibre channels. As the 64-bit @ 200 MHz CSIX interface's throughput is actually 1280 MB/s, in particular after removing overhead, it is unlikely that any bandwidth problem will occur.

3. Please insert the following new paragraph [0032a] after existing paragraph [0032]:

[0032a] In a further embodiment of the present invention, the bridge is coupled to a computer system or server via CPU interface 430. The CPU interface 430 may be coupled to a computer system or server via a bus, such as a PCI bus or other means known in the art.

4. Please replace paragraph [0037] with the following paragraph:

[0037] If the bridge is designed to be part of a robust system, the external memory interface can be equipped with error protection, such as parity or error correction code. Thus, to provide a highly reliable memory, for example, an error correcting code (ECC) memory can be used with the bridge according to the present invention. A first type of such a memory uses, for example but is not limited to, 1 check bit which is required to protect 8-bits of data. For a 128-bit memory interface, a total of 16 additional signals may be needed to provide memory protection for 128-bit of data resulting in a 144 bit wide data bus. Figure 5 depicts a possible arrangement including four QDR SRAM modules **510 (e.g., QDR SRAM 3, QDR SRAM 2, QDR SRAM 1, QDR SRAM 0)** and the coupling of, for example but is not limited to, 25 command, clock and address lines whereas Figure 6 depicts the coupling of the 144 data lines for the same arrangement. The coupling of the command lines may include optional registers as illustrated in Figure 5. These registers are used to latch data from DRAM devices. Typically, they are needed when the system operates at high speed data rate.